**Supplementary Information**

**Modulation of magnetoresistance polarity in BLG/SL-MoSe2 heterostacks**

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**Supplementary Note 1. Fabrication of hole through wafers**

All devices were made using few-steps fabrication process as shown schematically in Supplementary Note 4. To make hole across the wafers, (SiN-300 nm/SiO2-300 nm/Si-600 m/SiO2-300 nm/SiN-300 nm), we followed some steps with sequence. First of all, in 1st step the LOR and photoresist (S1813) were spin-coated from the back side of the wafer to make 40 x 40 m square by using photolithography. The SiN-300 nm was removed from this square area by inductively coupled plasma (ICP) dry etching system with CH3F4 gas plasma and following SiO2-300 nm was etched by using buffer oxide etchant (BOE) for 5 minutes. Subsequently, the Si-600 m was etched by wet chemical method in which Si was exposed to KOH aqueous solution at 80 0C until the top SiO2-300 nm is not revealed. Meanwhile after washing with distill water we dried the wafer by N2 blow carefully. Further in 2nd step the upper SiO2-300 nm layer was again removed by BOE to render top thick free-standing SiN- 300 nm window. Finally, we spin coated the ZEP polymer on top of wafer for electron beam lithography to drill hole through suspended SiN membrane, thereby after e.beam lithography we expose circular hole area (~1 m radius) by developing and etched by using again CH3F4 gas plasma. Later on, we wash and clean the wafer in hot PG remover and isopropyl alcohol (IPA). To ensure good adhesion between 2D material and SiN we did oxygen plasma by ICP to attain cleaner SiN surface particularly around hole. Eventually, the thick h-BN flake (necessary for only single layer graphene adhesion, otherwise SiN is not best option) was transferred on top of SiN hole by PMMA membrane and annealed on hot plate at 200 0C for 2 min. Meanwhile, the reactive ion etching (RIE) was done from the back side of the wafer with CF4 plasma to etch h-BN completely from the suspended part. Simultaneously, the SiN membrane etched from the back side become thinner upto ~150 nm which is enough to suspend 2D materials and washed our devices in acetone to remove PMMA. Ultimately in 3rd step the single layer graphene, larger than hole size, was transferred onto hole through h-BN by PMMA membrane. At this critical point, to remove PMMA we put our devices vertically in hot acetone and IPA. By using this strategy our efficiency to attain stable suspended single layer graphene is 99.9 %. Further, we annealed the devices in mixture of N2 and H2 gasses environment at 350 0C for 4 hours to get rid from polymer residue. Finally, the Co and NiFe are deposited at top and from bottom of the suspended graphene, respectively.

**Supplementary Note 2. Schematic illustration of device fabrication for hole**



1st step



2nd step



3rd step



**Figure S1. Characterizations of suspended graphene structure**. **(a)** The Raman spectrum of bilayer suspended graphene. The small D peak is observed which attributed to strain effect and is normal in suspended graphene. **(b)** After FMs depositions the Scanning electron microscopy (SEM) image of final device from top side.



**Figure S2. (a)** The AFM image of single layer MoSe2 flake is taken on substrate. **(b)** The height profile corresponding to thin MoSe2 shows single layer as the thickness of our flake is very close to reported value (~0.77 nm). **(c)** The Raman spectrum of single layer MoSe2 on supported region. The A1g and E12g peaks are observed around ~240.6 and 286.4 cm-1 which is also sign of single layer MoSe2.







**Figure S3. (a)** Schematic drawing of graphene FETs with Co and NiFe doping. **(b)** The resistivity *vs* back gate, Dirac measurements. **(c)** The RA of the junction devices before and after annealing. The resistance of all devices is reduced after annealing.



**Figure S4**. The MR (%) values at different temperature for all type of devices after annealing by keeping current I = 10 A.