# **Device fabrication**

The top and bottom chips of our device is fabricated in a cleanroom using standard photolithography, wet etching processes as shown in Fig. 2. Indium Tin Oxide (ITO) or chromium coated glass substrates are used as the top and bottom plates. The process starts with cleaning the wafer thoroughly with non-halogenated hydrocarbons: Acetone, Methanol, Isopropanol and then rinsing with DI water followed by a dehydration process at 150 0C for 5 minutes. For the bottom chip, at first, HMDS is spin coated with the following recipe: speed of 500 rpm with a ramping rate of 100 rpm/s for 5 s; ramping with 900 rpm/s to 4000 rpm for 30s. The thin HMDS layer provides good adhesion between the ITO layer and the photoresist which will be deposited next. After the coating, the wafer is baked at 1500 C for 3 minutes. Next, a positive PR (Microchem S1813) is spin coated on the wafer with following recipe; spin speed 500 rpm with ramping rate of 100 rpm/s for 5s; ramping with 900 rpm/s to 3000 rpm for 30s. This results in a uniform 1.2 μm thick PR layer. The glass substrate with the coated PR layer is then baked at 120 0C for 2 minutes. The PR is then exposed to UV light with a dose of 140 mJ/cm2 on the Backside-Aligner (OAI 806MBA) followed by a baking step at 115 0C for 1 minute 30 s. After that, the wafer is dipped in a developer (Microchem, MF-319) bath for 1 minute and then rinsed thoroughly with water and dehydrated. The resulted electrode pattern is checked under the microscope for accuracy. The wafer is then dipped in a mixture of Hydrochloric (HCL) acid, Nitric (HNO3) acid and DI water (H2O) (wt %- 20% HCl, 5% HNO3, 75% H2O or vol %- 8:1:15, HCl: HNO3: H2O) for 2.5 minutes at 55 0C to etch the conductive ITO layer. If chromium is used as the conductive layer, the wafer is dipped into chromium etchant bath for 3 minutes to pattern the electrodes. After etching, the PR layer is PR stripped with PR stripper (Remover 1165, Microchem), then the wafer is dehydrated at 150 0C for 5 min. Next, to provide an insulation layer, a dielectric material (SU-8-5, Microchem) is spin coated on the wafer with following recipe; spin speed of 500 rpm with a ramping rate of 100 rpm/s for 5s; spin speed 2000 rpm with a ramping rate of 900 rpm/s for 30s) resulting in a 5 μm thick uniform dielectric layer. It is then baked to harden the layer at 65 0C for 1 minute and then 95 0C for 3 minutes. For hardening the layer, it is exposed to UV light with a light dose of 140 mJ/cm2 on the Backside-Aligner (OAI 806MBA). The wafer is then soft baked at 65 0C for 1 minute, 95 0C for 1 minute and hard backed at 150 0C for 5 minutes. A hydrophobic layer is then created by spin coating a 300 nm thick uniform Teflon layer with the following recipe: spin speed of 1000 rpm with a ramping rate of 300 rpm/s for 30s. For the top chip, an ITO coated cover plate is first cleaned thoroughly with non-halogenated hydrocarbons: Acetone, Methanol, Isopropanol and then rinsed with DI water. It is then dehydrated at 150 0C for 5 minutes. A 300 nm thick Teflon layer is deposited using the same recipe as described before.